CLAIMS

1. (Currently Amended-Withdrawn) A first-in-first-out memory, comprising:

a memory array having an array of single port memory cells;

a clock terminal ~~for receiving~~ that receives a clock signal;

a write enable terminal ~~for receiving~~ that receives a write enable signal;

inputs ~~for receiving~~ that receives input data words;

a read enable terminal ~~for receiving~~ that receives a read enable signal;

outputs ~~for presenting~~ that presents output data words of the same word width as that of the input data words;

a write buffer[[,]] that is coupled to the inputs and to the array of memory cells, ~~for receiving~~ that receives a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal, ~~and for writing~~ wherein the write buffer performs a first width conversion of the first and second input data words to the memory array in a single write cycle;

read circuitry~~, for requesting~~ that requests a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and

a read buffer~~, for receiving~~ that receives first and second output data words from the memory array responsive to the request of the read of the memory array, and ~~for presenting~~ that presents the first and second output data words in sequence to the outputs.

2. (Currently Amended-Withdrawn) The memory circuit of claim 1, wherein the write buffer comprises:

a plurality of buffer storage locations; and

sequential logic~~, for controlling~~ that controls the write buffer to store input data words received from the inputs in selected ones of the buffer storage locations, and ~~for controlling~~ that controls the write buffer to forward pairs of stored input data words to the memory array.

3. (Currently Amended-Withdrawn) The memory circuit of claim 2, wherein the plurality of buffer storage locations are arranged in rows and columns, including first

and second columns of the buffer storage locations ~~having~~ that have storage locations in first and second rows.

4. (Currently Amended-Withdrawn) The memory circuit of claim 3, wherein the sequential logic controls the write buffer to store a first input data word in a buffer storage location at the first row and the first column[[,]] and to store a second input data word in a buffer storage location at the second row and the first column[[:]], and wherein the sequential logic ~~also~~ controls the write buffer to then forward the first and second input data words to the memory array in an internal write cycle.

5. (Currently Amended-Withdrawn) The memory circuit of claim 4, wherein the memory circuit further ~~comprising~~ comprises:

a clock input ~~for receiving~~ that receives a periodic clock signal; and

clock circuitry~~, for assigning~~ that assigns alternating cycles of the periodic clock signal as internal write and internal read cycles.

6. (Currently Amended-Withdrawn) The memory circuit of claim 5, wherein the sequential logic ~~also~~ controls the write buffer to then store a third input data word in a buffer storage location of the second column responsive to the inputs receiving the third input data word prior to an internal write cycle.

7. (Currently Amended-Withdrawn) The memory circuit of claim 1, wherein the read buffer comprises:

an output width converter~~, for converting~~ that converts double-width output data words read from the memory array into a sequence of output data words; and

an output First-In-First-Out (FIFO)[[,]] that is coupled to the output width converter~~, for buffering the output data words in a first-in-first-out fashion~~.

8. (Currently Amended-Withdrawn) The memory circuit of claim 7, wherein the read circuitry further comprises[[:]] an output register ~~for presenting~~ that presents an

output data word received from the output FIFO at the outputs, in combination with a data valid signal, responsive to the read circuitry receiving a read enable signal.

9. (Currently Amended-Withdrawn) The memory circuit of claim 7, wherein the output FIFO generates a read ready signal responsive to its contents, wherein the output FIFO stores ~~storing~~ a number of output data words exceeding a first threshold.

10. (Currently Amended-Withdrawn) The memory circuit of claim 9, wherein the output FIFO generates a stop read signal to the memory array responsive to its contents storing a number of output data words exceeding a second threshold that is higher than the first threshold[[;]], and wherein the output FIFO generates a start read signal to the memory array responsive to its contents, and wherein the output FIFO stores ~~storing~~ a number of output data words below a third threshold that is lower than the first threshold.

11. (Currently Amended-Withdrawn) The memory circuit of claim 1, wherein the input data words and output data words correspond to data arranged in packets, each packet including a start-of-packet indicator and an end-of-packet indicator[[;]], and wherein the memory circuit further ~~comprising:~~ comprises packet management logic~~, for controlling~~ that controls the operation of the memory circuit, the packet management logic for enabling the outputting of output data words corresponding to a packet, responsive to detecting the writing of a start-of-packet indicator and an end-of-packet indicator.

12. (Currently Amended-Withdrawn) The memory circuit of claim 12, wherein the packet management logic ~~is also for enabling~~ enables the outputting of output data words corresponding to a jumbo packet, responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold.

13. (Currently Amended-Withdrawn) The memory circuit of claim 11, wherein the packet management logic ~~is also for maintaining~~ maintains a count of the number of packets stored in the memory array.

14. (Currently Amended-Withdrawn) The memory circuit of claim 13, wherein the packet management logic ~~is also for disabling~~ disables the outputting of output data words, responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored.

15. (Currently Amended-Withdrawn) The memory circuit of claim 14, wherein the read buffer comprises:

an output width converter~~, for converting~~ that converts double-width output data words read from the memory array into a sequence of output data words;

an output FIFO, coupled to the output width converter~~, for buffering the output data words in a first-in-first-out fashion~~; and

an output register ~~for presenting~~ that presents an output data word received from the output FIFO at the outputs, in combination with a data valid signal, responsive to the read circuitry receiving a read enable signal[[.]], and wherein the packet management logic controls the output register to disable the outputting of output data words responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored.

16. (Currently Amended-Withdrawn) A method of buffering data words with a memory circuit having an array of single port memory cells, the method comprising the steps of:

receiving a sequence of input data words at input terminals of the memory circuit;

responsive to receiving a first input data word and a second input data word, ~~writing~~ performing a first width conversion of the first and second input data words into a memory array of the memory circuit in a single write cycle;

receiving read strobe signals;

responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle;

performing a second width conversion of the first and second output data words; and

sequentially presenting the first and second output data words at output terminals of the memory circuit, wherein the first and second output data words are of the same word width as that of the input data words.

17. (Currently Amended-Withdrawn) The method of claim 16, wherein the method further ~~comprising:~~ comprises responsive to receiving an input data word, storing the input data word in a write buffer having a plurality of buffer storage locations arranged in rows and columns, each column having first and second buffer storage locations associated with first and second rows, respectively~~; and,~~ wherein the ~~writing~~ step of performing the first width conversion is performed responsive to the first and second buffer storage locations of a first column storing the first and second input data words, respectively.

18. (Currently Amended-Withdrawn) The method of claim 17, wherein the method further ~~comprising~~ comprises:

receiving a periodic system clock signal; and

assigning internal write cycles and internal read cycles to alternating ones of an internal clock corresponding to the system clock signal.

19. (Currently Amended-Withdrawn) The method of claim 18, wherein the ~~writing~~ step of performing the first width conversion is performed responsive to the first and second buffer storage locations of the first column storing the first and second input data words, respectively, in combination with an internal write cycle.

20. (Currently Amended-Withdrawn) The method of claim 19, wherein the method further ~~comprising~~ comprises:

receiving a third input data word; and

responsive to receiving the third input data word and to the first and second buffer storage locations of the first column storing the first and second input data words, respectively, and prior to an internal write cycle, storing the third input data word in a buffer storage location of a second column.

21. (Currently Amended-Withdrawn) The method of claim 16, wherein the method further ~~comprising~~ comprises:

after the reading step and prior to the presenting step, buffering the first and second output data words in an output FIFO buffer; and

before the presenting step, generating a read ready signal responsive to the output FIFO buffer storing a number of output data words exceeding a first threshold[[;]], and wherein the presenting step is performed responsive to receiving a read strobe signal after the generating of the read ready signal.

22. (Currently Amended-Withdrawn) The method of claim 21, wherein the method further ~~comprising~~ comprises:

generating a stop read signal to the memory array responsive to the output FIFO buffer storing a number of output data words exceeding a second threshold that is higher than the first threshold; and

generating a start read signal to the memory array responsive to the output FIFO buffer storing a number of output data words below a third threshold that is lower than the first threshold.

23. (Currently Amended) A method of managing the communications of data words arranged in packets, each packet of data words including a start-of-packet indicator and an end-of-packet indicator[[;]], the method comprising:

receiving a sequence of input data words at input terminals of the memory circuit;

responsive to receiving a first input data word and a second input data word, ~~writing~~ performing a first width conversion of the first and second input data words into a memory array of the memory circuit in a single write cycle;

responsive to detecting the writing of input data words including a start-of-packet indicator and of an end-of-packet indicator, enabling the output of data words corresponding to the packet;

receiving read strobe signals;

responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle;

performing a second width conversion of the first and second output data words; and

sequentially presenting the first and second output data words at output terminals of the memory circuit, wherein the first and second output data words are of the same word width as that of the input data words.

24. (Currently Amended) The method of claim 23, wherein the method further ~~comprising:~~ comprises enabling the output of data words corresponding to the packet, responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold.

25. (Currently Amended) The method of claim 23, wherein the method further ~~comprising:~~ comprises incrementing a count of the number of packets stored in the memory array responsive to detecting the writing of an end-of-packet indicator.

26. (Currently Amended) The method of claim 25, wherein the method further ~~comprising~~ comprises disabling the outputting of output data words, responsive to the outputting of an end-of-packet indication for a packet and to the count indicating that no additional packets are stored.

27. (Currently Amended) The method of claim 26, wherein the disabling step comprises[[:]] controlling an output register to disable the presenting of output data words at the output terminals.

28. (Currently Amended) A network node for controlling the transmission and receipt of packet-based data over a communications facility[[,]] comprising:

a system interface ~~for receiving~~ that receives transmit data from a system and for outputting processed received signals to the system;

a transmit FIFO buffer~~, for buffering~~ that buffers transmit data received at the system interface;

a transceiver~~, for driving~~ that drives the communications facility with transmitted signals corresponding to the transmit data[[,]] and ~~for receiving~~ that receives signals from the communications facility; and

a receive FIFO buffer~~, for buffering~~ that buffers the received signals~~; and,~~ wherein each of the transmit and receive FIFO buffers ~~comprise~~ include:

a memory array;

a clock terminal ~~for receiving~~ that receives a clock signal;

a write enable terminal ~~for receiving~~ that receives a write enable signal;

inputs ~~for receiving~~ that receive input data words;

a read enable terminal ~~for receiving~~ that receives a read enable signal;

outputs ~~for presenting~~ that presents output data words of the same word width as that of the input data words;

a write buffer[[,]] that is coupled to the inputs and to the array of memory cells~~, for receiving~~ and that receives a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal, ~~and for writing~~ wherein the write buffer performs a first width conversion of the first and second input data words to the memory array in a single write cycle;

read circuitry~~, for requesting~~ that requests a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and

a read buffer~~, for receiving~~ that receives first and second output data words from the memory array responsive to the request of the read of the memory array[[,]]

and ~~for presenting~~ that presents the first and second output data words in sequence to the outputs.

29. (Currently Amended) The network node of claim 28, wherein the transceiver further comprises:

a serializer~~, for serializing~~ that serializes the transmit data;

a line driver~~, for driving~~ that drives the communications facility with serial signals from the serializer;

a receiver~~, for receiving~~ that receives serial signals from the communications facility; and

a deserializer~~, for deserializing~~ that deserializes the signals received by the receiver.

30. (Currently Amended) The network node of claim 28, wherein the network node further ~~comprising~~ comprises:

a transmit media access control function~~, for processing~~ that processes the transmit data buffered by the transmit FIFO buffer; and

a receive media access control function~~, for processing~~ that processes the received signals and ~~applying~~ that applies the processed received signals to the receive FIFO buffer.

31. (Currently Amended) The network node of claim 28, wherein the write buffer in each of the transmit and receive FIFO buffers further comprises:

a plurality of buffer storage locations arranged in rows and columns, including first and second columns of buffer storage locations having storage locations in first and second rows; and

sequential logic~~, for controlling~~ that controls the write buffer to store a first input data word in a buffer storage location at the first row and the first column, ~~and~~ to store a second input data word in a buffer storage location at the second row and the first column, and to then forward the first and second input data words to the memory array in an internal write cycle.

32. (Currently Amended) The network node of claim 31, wherein the write buffer in each of the transmit and receive FIFO buffers further comprises:

a clock input ~~for receiving~~ that receives a periodic clock signal; and

clock circuitry~~, for assigning~~ that assigns alternating cycles of the periodic clock signal as internal write and internal read cycles[[;]], wherein the sequential logic ~~also~~ controls the write buffer to then store a third input data word in a buffer storage location of the second column responsive to the inputs receiving the third input data word prior to an internal write cycle.

33. (Currently Amended) The network node of claim 28, wherein the read buffer in each of the transmit and receive FIFO buffers further comprises:

an output width converter~~, for converting~~ that converts double-width output data words read from the memory array into a sequence of output data words; and

an output FIFO[[,]] that is coupled to the output width converter~~, for buffering the output data words in a first-in first-out fashion~~.

34. (Currently Amended) The network node of claim 33, wherein the read circuitry further comprises[[:]] an output register ~~for presenting~~ that presents an output data word received from the output FIFO at the outputs, in combination with a data valid signal, responsive to the read circuitry receiving a read enable signal.

35. (Original) The network node of claim 33, wherein the output FIFO generates a read ready signal responsive to its contents storing a number of output data words exceeding a first threshold.

36. (Cancelled)

37. (Currently Amended) The network node of claim 28, wherein each packet of data words includes a start-of-packet indicator and an end-of-packet indicator[[;]], and wherein each of the transmit and receive FIFO buffers further comprises[[:]] packet

management logic~~, for controlling~~ that controls the operation of the memory circuit~~, the packet management logic for enabling~~ and that enables the outputting of output data words corresponding to a packet, responsive to detecting the writing of a start-of-packet indicator and an end-of-packet indicator.

38. (Currently Amended) The network node of claim 37, wherein the packet management logic ~~is also for enabling~~ enables the outputting of output data words corresponding to a jumbo packet, responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold.

39. (Currently Amended) The network node of claim 37, wherein the packet management logic ~~is also for maintaining~~ maintains a count of the number of packets stored in the memory array.

40. (Currently Amended) The network node of claim 39, wherein the packet management logic ~~is also for disabling~~ disables the outputting of output data words, responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored.

41. (Currently Amended) The network node of claim 40, wherein the read buffer further comprises:

an output width converter~~, for converting~~ that converts double-width output data words read from the memory array into a sequence of output data words;

an output FIFO[[,]] that is coupled to the output width converter~~, for buffering the output data words in a first-in first-out fashion~~; and

an output register ~~for presenting~~ that presents an output data word received from the output FIFO at the outputs, in combination with a data valid signal, responsive to the read circuitry receiving a read enable signal[[.]], and wherein the packet management logic controls the output register to disable the outputting of output data words responsive to the

outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored.